AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously presented) A multilayer semiconductor device assembly jig, comprising:

a lateral position restriction mechanism for positioning a plurality of stacked semiconductor modules on a base member with their respective lateral positions mutually restricted;

a height restriction mechanism for restricting an entire height of said semiconductor modules layered on said base member; and

an alignment mechanism for providing alignment with reference to a mother substrate and further wherein a plurality of the semiconductor modules are each comprised of a single semiconductor chip secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein a plurality of adjacent printed wiring board members are secured to one another by solder connections between top and bottom surfaces thereof.

2. (Original) The multilayer semiconductor device assembly jig according to claim 1 comprising a box-shaped member which is positioned on said base member and having a storage space for storing said semiconductor modules in a layered state,

wherein an inner wall of said storage space constitutes said lateral position restriction mechanism.

3. (Original) The multilayer semiconductor device assembly jig according to claim 2, wherein said alignment mechanism comprises a plurality of positioning pins and positioning holes for receiving the positioning pins which are correspondingly formed in said box-shaped member and said mother substrate.

4. (Original) The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins secured in said base member and which are used for securing at least three different portions of an outer periphery of said semiconductor modules.

5. (Previously Presented) The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins secured in said base member and which pierce through positioning holes formed in said semiconductor modules.

6. (Currently Amended) The multilayer semiconductor device assembly jig according to claim 5, wherein said positioning pins also pierce through a positioning hole formed ~~on~~ in said mother substrate.

7. (Original) The multilayer semiconductor device assembly jig according to claim 1, wherein said height restriction mechanism further comprises:

a cover member secured over said semiconductor modules.

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (New) A multilayer semiconductor device assembly jig, comprising:

a lateral position restriction mechanism for positioning a plurality of stacked semiconductor modules on a base member with their respective lateral positions mutually restricted, the lateral position restriction mechanism comprised of two opposed side walls having a single stack of the semiconductor modules therebetween;

a height restriction mechanism for restricting an entire height of said semiconductor modules layered on said base member, said height restriction mechanism being located directly above the stacked semiconductor modules; and

an alignment mechanism for providing alignment with reference to a mother substrate and further wherein a plurality of the semiconductor modules are each comprised of a single semiconductor chip secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein a plurality of adjacent printed wiring board members are secured to one another by solder connections between top and bottom surfaces thereof.

12. (New) The multilayer semiconductor device assembly jig of claim 11, wherein the alignment mechanism is comprised of a plurality of vertical pins arranged adjacent and in contact with sides of the stacked semiconductor modules.

13. (New) The multilayer semiconductor device assembly jig of claim 11, wherein the alignment mechanism is comprised of a plurality of vertical pins that extend through the stacked semiconductor modules.